INTERRUPTING A MICROPROCESSOR ONLY AFTER A TRANSACTION IS COMPLETE

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ABSTRACT

A network device includes a first port to allow the device to communicate with other devices on an expansion bus. The device also includes a second port to allow the device to communicate with devices on a second bus and a memory to store data. A processor receives an interrupt signal from an expansion device on the expansion bus and generates an indicator of completion. The processor then inserts the indicator into a transaction queue after the set of data.